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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* JAE-JUN MOON, JEONG-WON LEE,
and JUNG-EUN LEE

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Appeal 2008-2203
Application 10/777,097
Technology Center 2800

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Decided: July 29, 2008

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Before KENNETH W. HAIRSTON, ROBERT E. NAPPI, and KARL D. EASTHOM *Administrative Patent Judges.*

NAPPI, *Administrative Patent Judge.*

## DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 6(b) of the final rejection of claims 1 through 10.

We affirm the Examiner's rejections of these claims.

## INVENTION

The invention is directed to a bias circuit that has a current mirror and a start up circuit. See pages 1 and 2 of Appellants' Specification. Claim 1 is representative of the invention and reproduced below:

1. A bias circuit having a start-up circuit, comprising:
a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and
a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

## REFERENCES

| | | |
|---|---|---|
| Yamazaki | US 5,180,967 | Jan. 19, 1993 |
| Wu | US 5,307,007 | Apr. 26, 1994 |

## REJECTIONS AT ISSUE

Claims 1, 3, and 5 through 9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wu. The Examiner's rejection is on pages 3 and 4 of the Answer.

Claims 1 through 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Wu. The Examiner's rejection is on pages 4 through 6 of the Answer.

Throughout the opinion, we make reference to the Brief (received April 20, 2007), Reply Brief (received October 3, 2007) and the Answer (mailed August 3, 2007) for the respective details thereof.

## ISSUES

*Rejection under 35 U.S.C. § 102(b)*

Appellants argue on pages 11 through 13 of the Brief that the Examiner's rejection of claims 1, 3, and 5 through 9 under 35 U.S.C. § 102(b) is in error. Appellants argue that Wu does not teach an output node

as claimed. Brief 11. Appellants assert the Examiner's finding that the node between transistors M1 and M3 is an output node is in error, stating "there is absolutely nothing at the gate of the NMOS transistor M3 which would allow the output or the detection of any voltage at the gate." Brief 12.

Thus, Appellants' contentions with respect to the rejection of claims 1, 3, and 5 through 9 under 35 U.S.C. § 102(b) present us with the issue of whether the Examiner erred in finding that Wu teaches an output node as claimed.

*Rejection under 35 U.S.C. § 103(a)*

Appellants argue on pages 14 through 17 of the Brief that the Examiner's rejection of claims 1 through 10 under 35 U.S.C. § 103(a) is in error. Appellants argue that the combination of Yamazaki and Wu does not teach the claimed output node. Appellants assert that the Examiner erroneously equated the nodes N11 and N12 as output nodes. Brief 14. Appellants further argue that the Examiner's reasoning for combining the references is based upon hindsight reasoning and that there is nothing in Yamazaki which suggests generating a constant output voltage as claimed. Brief 14- 15.

With respect to dependent claim 4, Appellants additionally argue that Yamazaki does not teach the first NMOS transistor connected to the third PMOS transistor as claimed.

Thus, Appellants' arguments with respect to the rejection of claims 1 through 10 under 35 U.S.C. § 103(a) present us with several issues. First did the Examiner err in determining that the combination of Yamazaki in view of Wu teaches an output node as claimed, and second did the Examiner err in combining the references? With respect to claim 4, Appellants'

contentions present us with the additional issue of whether the Examiner erred in finding that the combination of the references teaches the connection between the first NMOS transistor and the third PMOS transistor as claimed.

## PRINCIPLES OF LAW

In analyzing the scope of the claim, Office personnel must rely on Appellant's disclosure to properly determine the meaning of the terms used in the claims. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995). "[I]nterpreting what is *meant* by a word *in* a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.'" (Emphasis original) *In re Cruciferous Sprout Litigation,* 301 F.3d 1343, 1348 (Fed. Cir. 2002) (citing *Intervet Am. Inc. v. Kee-Vet Labs. Inc.,* 887 F.2d 1050, 1053 (Fed. Cir. 1989)).

37 C.F.R. § 41.37 (c)(1)(vii) states:

> For each ground of rejection applying to two or more claims, the claims may be argued separately or as a group. When multiple claims subject to the same ground of rejection are argued as a group by appellant, the Board may select a single claim from the group of claims that are argued together to decide the appeal with respect to the group of claims as to the ground of rejection on the basis of the selected claim alone. Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.... A statement which merely points out what a claim recites will not be considered an argument for separate patentability of the claim.

On the issue of obviousness, the Supreme Court has recently stated that "the obviousness analysis cannot be confined by a formalistic

conception of the words teaching, suggestion, and motivation." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007). Further, the Court stated "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1739 (2007).

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. . . . [A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

*Id.* at 1740. "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims." *Id.* at 1742.

## FINDINGS OF FACT

1. Wu teaches transistors M1 and M2 create a current mirror (item 20). Col. 3, ll. 28-29.
2. This current mirror works with another current mirror (item 10) made up of transistors M3-M6 to provide a stable current source independent of the voltage source change. Wu, col. 3, ll. 40-41.
3. As shown in figure 1 of Wu, the node between transistors M1 and M3 is also connected to the gates of transistors M3, M4, M5, and M6.

4. As transistors M4, M5, and M6 of Wu are slaved to voltage at the node between transistors M1 and M3 to provide a stable current source, it is apparent that the voltage output from this node is a constant bias voltage.
5. As also shown in figure 1 of Wu, a capacitor C1 is connected at one end to the node between transistors M1 and M3 and at the other end to the node connecting the gates of the MOS transistors M1 and M2 that make up the current mirror (item 20). This capacitor aids in start up of the current mirror. Wu, col. 3, ll. 47-48.
6. Yamazaki teaches a self activating current mirror circuit which makes use of two transistors (120, 118) to assist in start up of the current mirror. Abstract; col. 6, ll. 15-23.
7. In one embodiment of Yamazaki, a PMOS transistor 110 is connected through transistor 128 to the drain of PMOS transistor 126. See figure 5.

## ANALYSIS

*Rejection under 35 U.S.C. § 102(b)*

Initially, we note that Appellants do not separately argue any of the claims, thus, in accordance with 37 C.F.R. § 41.37 (c)(1)(vii), claims 1, 3, and 5 through 9 are grouped together. We select claim 1 as representative of the group of claims rejected under 35 U.S.C. § 102(b).

Appellants' arguments have not persuaded us of error in the Examiner's rejection of claims 1, 3, and 5 through 9 under 35 U.S.C. § 102(b). The Examiner finds that Wu, in figure 1, teaches a bias circuit, with a start up capacitor (item C1), an output node (between transistors M1

and M3) and a common node (at the gates of transistors M1 and M2).

Answer 3. Further, the Examiner finds that the node provides an output of a constant bias voltage that is input to the gates of transistors M5 and M6.

Answer 7. In response to Appellants' arguments the Examiner states:

> [Appellants'] Claim 1 is directed toward Appellant's [sic] Fig. 7, for example. Fig. 7 shows a slightly modified version of a well-known Wilson-type bias circuit as illustrated by Appellant's [sic] Prior Art Fig. 1. By itself, a bias circuit has no real-world value. Bias circuits are building-blocks that are used to create larger, usable electronic systems. One of ordinary skill in the art would recognize that the very purpose of a bias circuit is to provide or output a bias for extraction by another down-stream electronic component. The Wu et al. reference shows an example of a larger electronic system utilizing a Wilson-type bias circuit building-block for providing or outputting a constant bias voltage to down-stream components M5 and M6, for example. Although the node between M1 and M3 is internal to the larger electronic system, the node is, nevertheless, an output node of the Wilson-type bias sub-circuit. The output node between bias circuit transistors M1 and M3 is exactly the same as the output node REF or Vgn shown in Appellant's [sic] Fig. 1 or 7, respectively.

Answer 7 (emphasis original).

We concur with the Examiner's findings as we find that they are supported by the Evidence of record. Claim 1 recites a "bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node." Wu teaches that in the circuit of figure 1, the transistors M1 and M2 create a current mirror. Fact 1. The node between transistors M1 and M3 is also connected to the gates of transistors M3, M4, M5, and M6 and provides a constant bias voltage. Fact 3. Thus, we find that Wu teaches the first limitation of a constant bias circuit. Claim 1 further, recites a "start up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors

constructing the current mirror." Wu teaches a capacitor C1 connected in this manner. Fact 5. Thus, we find that Wu teaches the limitation of a start up circuit.

Appellants' arguments attempting to differentiate the output node from Wu's node between transistors M1 and M3 amount to a difference without a distinction. Appellants' Specification does not provide a special definition of the term output node. We construe this limitation as a node which provides an output to another circuit or a portion of the same circuit having a different function . As discussed above by the Examiner, bias circuits by their very nature are to provide an output to other circuits. That Wu depicts the circuits whereas Appellants chose not to depict or claim the additional circuits, does not differentiate the claim from Wu. Thus, Appellants' arguments have not persuaded us that the Examiner erred in finding that Wu teaches an output note as claimed. Accordingly, we sustain the Examiner's rejection of claims 1, 3, and 5 through 9 under 35 U.S.C. § 102(b).

*Rejection under 35 U.S.C. § 103(a)*

Initially, we note that Appellants only provide a separate argument with respect to claim 4. Thus, in accordance with 37 C.F.R. § 41.37 (c)(1)(vii), claims 1, 2, 3, and 5 through 10 are grouped together and we select claim 1 as representative of this group of claims rejected under 35 U.S.C. § 103(a).

Appellants' arguments have not persuaded us of error in the Examiner's rejection of claims 1, 2, 3, and 5 through 10 under 35 U.S.C. § 103(a). Initially, we note that as discussed above with respect to the rejection under 35 U.S.C. § 102(b), we find no error in the Examiner's

rejection of claim 1 as anticipated by Wu, thus for this reason alone we find no error in the rejection under 35 U.S.C. § 103(a), if Wu anticipates all of the limitations claim 1 it certainly makes them obvious.

Nonetheless, Appellants' arguments have not persuaded us that the Examiner erred in finding that node N11 of Yamazaki meets the claimed output node. In response to Appellants' arguments, the Examiner provides rationale and analysis similar to that discussed above with respect to the rejection under 35 U.S.C. § 102(b). Answer 9. We concur with the Examiner's analysis, as discussed above; we construe this limitation as a node which provides an output to another circuit or circuit portion. As is apparent from Yamazaki's figure 1, node N11 outputs a signal to the gate of transistor 116. In combination the Examiner finds that one skilled in the art would replace the start up circuits 118 and 120 of Yamazaki with the start up capacitor as taught by Wu. Answer 4-5.

Further, as the Examiner states, on page 10 of the Answer, that when combined with Wu:

> The portion of Appellant's [sic] circuit structure relevant to generating a constant voltage structure is identical to Yamazaki's structure relevant to generating a constant bias voltage. If Appellant's [sic] structure generates a constant bias voltage than the corresponding structure of Yamazaki circuit must also generate a constant bias voltage.

Answer 10.

We concur with the Examiner's reasoning. Appellants' argument on page 8 of the Reply Brief, that one combing the reference would place capacitor C1 between the common node connecting gates of transistors 112 and 110 and the node connecting transistors 104 and 106, has not persuaded us of error in the Examiner's rejection. Appellants' arguments overlook that

transistors 112 and 110 are also a current mirror and that the node between the gates of transistor 104 and 106 is the output node. Thus, Appellants' arguments have not persuaded us that the Examiner erred in determining that the combination of Yamazaki and Wu teach an output node as claimed.

Further, the Appellants' arguments have not persuaded us that the Examiner erred in combining the references. Here the Examiner demonstrated that Wu teaches use of a capacitor to assist in the start up of a current mirror circuit and that Yamazaki also teaches a circuit for starting up a current mirror. Facts 5 and 6. The combination by the Examiner substituting one start up circuit for another is nothing more than using known circuit arrangements for their intended purpose to yield predictable results. For the above reasons, Appellants have not persuaded us of error in the Examiner's rejection of claims 1, 2, 3, and 5 through 10 under 35 U.S.C. § 103(a).

Appellants' arguments directed to claim 4 have not persuaded us of error in the rejection of claim 4. Claim 4 recites "a first NMOS transistor having a drain and a gate thereof connected to a drain of the third PMOS transistor to form the output node." The Examiner, citing Yamazaki's figure 5, equates the first NMOS transistor with item 110, the second NMOS transistor with item 112, first PMOS transistor with item 106 and second PMOS transistor 104. Answer 5. Appellants argue, referring to figure 5 of Yamazaki, that the gate of NMOS transistor 110 is not connected to the drain of PMOS transistor 126, as transistor 128 is in between the two. Brief 16. In response, the Examiner states that the claim does not recite a direct connection between the drain and gate of the first NMOS transistor and the drain of the third PMOS transistor. Answer 11. Further, the Examiner

argues that there is no limitation which precludes transistor 128 from being between the two. Answer 11.

We concur with the Examiner's claim interpretation. Claim 4 is dependent upon claim 3 and recites a circuit comprising, meaning that the circuit may include elements not recited in the claims. Further, as the Examiner states, claim 4 does not recite a direct connection between the NMOS and PMOS transistors. We also concur with the Examiner's finding that the drain and gate of PMOS transistor 110, is connected through transistor 128 to the drain of PMOS transistor 126. Fact 7. Thus, Appellants' arguments have not persuaded us that the Examiner erred in finding that the combination of the references teaches the connection between the first NMOS transistor and the third PMOS transistor as claimed. Accordingly, we sustain the Examiner's rejection of claim 4.

## CONCLUSION

For the foregoing reasons, we sustain the Examiner's rejection of claims 1, 3, and 5 through 9 under 35 U.S.C. § 102(b) and the rejection of claims 1 through 10 under 35 U.S.C. § 103(a).

## ORDER

The decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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